

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRI-d encoded:
				5 *
				6 * E777 VSLDB - Vector Shift Left Double By Byte
				7 *
				8 * James Wekel March 2025
				9 *****
				11 *****
				12 *
				13 * basic instruction tests
				14 *
				15 *****
				16 * This program tests proper functioning of the z/arch E7 VRI-d
				17 * Vector Shift Left Double By Byt instruction.
				18 *
				19 * Exceptions are not tested.
				20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				22 * obvious coding errors. None of the tests are thorough. They are
				23 * NOT designed to test all aspects of any of the instructions.
				24 *
				25 *****
				26 *
				27 * *Testcase zvector-e7-20-VSLDB
				28 * *
				29 * * Zvector E7 instruction tests for VRI-d encoded:
				30 * *
				31 * * E777 VSLDB - Vector Shift Left Double By Byte
				32 * *
				33 * * # -----
				34 * * # This tests only the basic function of the instructions.
				35 * * # Exceptions are NOT tested.
				36 * * # -----
				37 * *
				38 * main size 2
				39 * numcpu 1
				40 * sysclear
				41 * archlvl z/Arch
				42 *
				43 * loadcore "\$(testpath)/zvector-e7-20-VSLDB.core" 0x0
				44 *
				45 * diag8cmd enable # (needed for messages to Hercules console)
				46 * runtest 2
				47 * diag8cmd disable # (reset back to default)
				48 *
				49 * *Done
				50 *
				51 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				53 *****
				54 * FCHECK Macro - Is a Facility Bit set?
				55 *
				56 * If the facility bit is NOT set, an message is issued and
				57 * the test is skipped.
				58 *
				59 * Fcheck uses R0, R1 and R2
				60 *
				61 * eg. FCHECK 134, 'vector-packed-decimal'
				62 *****
				63 MACRO
				64 FCHECK &BITNO, &NOTSETMSG
				65 . * &BITNO : facility bit number to check
				66 . * &NOTSETMSG : 'facility name'
				67 LCLA &FBBYTE Facility bit in Byte
				68 LCLA &FBBIT Facility bit within Byte
				69
				70 LCLA &L(8)
				71 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				72
				73 &FBBYTE SETA &BITNO/8
				74 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				75 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				76
				77 B X&SYSNDX
				78 * Fcheck data area
				79 * skip messgae
				80 SKT&SYSNDX DC C' Skipping tests: '
				81 DC C&NOTSETMSG
				82 DC C' (bit &BITNO) is not installed.'
				83 SKL&SYSNDX EQU *-SKT&SYSNDX
				84 * facility bits
				85 DS FD gap
				86 FB&SYSNDX DS 4FD
				87 DS FD gap
				88 *
				89 X&SYSNDX EQU *
				90 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				91 STFLE FB&SYSNDX get facility bits
				92
				93 XGR R0, R0
				94 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				95 N R0, =F' &FBBIT' is bit set?
				96 BNZ XC&SYSNDX
				97 *
				98 * facility bit not set, issue message and exit
				99 *
				100 LA R0, SKL&SYSNDX message length
				101 LA R1, SKT&SYSNDX message address
				102 BAL R2, MSG
				103
				104 B EOJ
				105 XC&SYSNDX EQU *
				106 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				108	*****
				109	* Low core PSWs
				110	*****
00000000		00000000	000013DB	111	ZVE7TST START 0
		00000000		112	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	113	
				114	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	116	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			117	DC X' 0000000180000000'
000001A8	00000000 00000200			118	DC AD(BEGIN)
000001B0		000001B0	000001D0	120	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			121	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			122	DC AD(X' DEAD')
000001E0		000001E0	00000200	124	ORG ZVE7TST+X' 200' Start of actual test program..
				126	*****
				127	* The actual "ZVE7TST" program itself...
				128	*****
				129	*
				130	* Architecture Mode: z/Arch
				131	* Register Usage:
				132	*
				133	* R0 (work)
				134	* R1- 4 (work)
				135	* R5 Testing control table - current test base
				136	* R6- R7 (work)
				137	* R8 First base register
				138	* R9 Second base register
				139	* R10 Third base register
				140	* R11 E7TEST call return
				141	* R12 E7TESTS register
				142	* R13 (work)
				143	* R14 Subroutine call
				144	* R15 Secondary Subroutine call or work
				145	*
				146	*****
00000200		00000200		148	USING BEGIN, R8 FIRST Base Register
00000200		00001200		149	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		150	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			152	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			153	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			154	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	156	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	157	LA R9, 2048(, R9) Inititalize SECOND base register
				158	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000020E	41A0 9800		00000800	159	LA	R10, 2048(, R9)	Initialize THIRD base register
00000212	41A0 A800		00000800	160	LA	R10, 2048(, R10)	Initialize THIRD base register
				161			
00000216	B600 828C		0000048C	162	STCTL	R0, R0, CTLR0	Store CR0 to enable AFP
0000021A	9604 828D		0000048D	163	OI	CTLR0+1, X' 04'	Turn on AFP bit
0000021E	9602 828D		0000048D	164	OI	CTLR0+1, X' 02'	Turn on Vector bit
00000222	B700 828C		0000048C	165	LCTL	R0, R0, CTLR0	Reload updated CR0
				166			
				167	*****		
				168	* Is z/Architecture vector facility installed (bit 129)		
				169	*****		
				170			
00000226	47F0 80A8		000002A8	171	FCHECK	129, 'z/Architecture vector facility'	
				172+	B	X0001	
				173+*			Fcheck data area
				174+*			skip messgae
0000022A	40404040 E2928997			175+SKT0001	DC	C'	Skipping tests: '
0000023E	A961C199 838889A3			176+	DC	C' z/Architecture vector facility'	
0000025C	404D8289 A340F1F2			177+	DC	C' (bit 129) is not installed.'	
		0000004E	00000001	178+SKL0001	EQU	*- SKT0001	
				179+*			facility bits
00000278	00000000 00000000			180+	DS	FD	gap
00000280	00000000 00000000			181+FB0001	DS	4FD	
000002A0	00000000 00000000			182+	DS	FD	gap
				183+*			
		000002A8	00000001	184+X0001	EQU	*	
000002A8	4100 0004		00000004	185+	LA	R0, ((X0001- FB0001)/8) - 1	
000002AC	B2B0 8080		00000280	186+	STFLE	FB0001	get facility bits
000002B0	B982 0000			187+	XGR	R0, R0	
000002B4	4300 8090		00000290	188+	IC	R0, FB0001+16	get fbit byte
000002B8	5400 8294		00000494	189+	N	R0, =F' 64'	is bit set?
000002BC	4770 80D0		000002D0	190+	BNZ	XC0001	
				191+*			
				192+*	facility bit not set, issue message and exit		
				193+*			
000002C0	4100 004E		0000004E	194+	LA	R0, SKL0001	message length
000002C4	4110 802A		0000022A	195+	LA	R1, SKT0001	message address
000002C8	4520 81A8		000003A8	196+	BAL	R2, MSG	
000002CC	47F0 8270		00000470	197+	B	EOJ	
		000002D0	00000001	198+XC0001	EQU	*	

[illegible]

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				331 *****
				332 * Normal completion or Abnormal termination PSWs
				333 *****
00000460	00020001 80000000			335 E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
00000470	B2B2 8260		00000460	337 E0J LPSWE E0JPSW Normal completion
00000478	00020001 80000000			339 FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
00000488	B2B2 8278		00000478	341 FAILTEST LPSWE FAILPSW Abnormal termination
				343 *****
				344 * Working Storage
				345 *****
0000048C	00000000			347 CTLR0 DS F CRO
00000490	00000000			348 DS F
00000494				350 LTORG , Literals pool
00000494	00000040			351 =F' 64'
00000498	000013B8			352 =A(E7TESTS)
0000049C	00000001			353 =F' 1'
000004A0	0000			354 =H' 0'
000004A2	005F			355 =AL2(L' MSGMSG)
				356
				357 * some constants
				358
	00000400	00000001		359 K EQU 1024 One KB
	00001000	00000001		360 PAGE EQU (4*K) Size of one page
	00010000	00000001		361 K64 EQU (64*K) 64 KB
	00100000	00000001		362 MB EQU (K*K) 1 MB
				363
	AABBCCDD	00000001		364 REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		365 REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				408	*****
				409	* E7TEST DSECT
				410	*****
				412	E7TEST DSECT ,
00000000	00000000			413	TSUB DC A(0) pointer to test
00000004	0000			414	TNUM DC H' 00' Test Number
00000006	00			415	DC X' 00'
00000007	00			416	I4 DC HL1' 00' i4 field
				417	
00000008	40404040	40404040		418	OPNAME DC CL8' ' E7 name
00000010	00000000			419	V2ADDR DC A(0) address of v2 source
00000014	00000000			420	V3ADDR DC A(0) address of v3 source
00000018	00000000			421	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			422	READRR DC A(0) result (expected) address
00000020	00000000	00000000		423	DS FD gap
00000028	00000000	00000000		424	V10OUTPUT DS XL16 V1 Output
00000038	00000000	00000000		425	DS FD gap
				426	
				427	* test routine will be here (from VRI-d macro)
				428	*
				429	* followed by
				430	* EXPECTED RESULT
				432	ZVE7TST CSECT ,
000010B4		00000000	000013DB	433	DS 0F
				435	*****
				436	* Macros to help build test tables
				437	*****
				439	*
				440	* macro to generate individual test
				441	*
				442	MACRO
				443	VRI_D &INST, &I4
				444	. * &INST - VRI-d instruction under test
				445	. * &I4 - shift
				446	
				447	GBLA &TNUM
				448	&TNUM SETA &TNUM+1
				449	
				450	DS 0FD
				451	USING *, R5 base for test data and test routine
				452	
				453	T&TNUM DC A(X&TNUM) address of test routine
				454	DC H' &TNUM test number
				455	DC X' 00'
				456	DC HL1' &I4' i4 field
				457	DC CL8' &INST' instruction name
				458	DC A(RE&TNUM+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				459	DC	A(RE&TNUM+32)	address of v3 source
				460	DC	A(16)	result length
				461	REA&TNUM	DC A(RE&TNUM)	result address
				462	DS	FD	gap
				463	V10&TNUM	DS XL16	V1 output
				464	DS	FD	gap
				465	. *		
				466	*		
				467	X&TNUM	DS OF	
				468	LGF	R1, V2ADDR	load v2 source
				469	VL	v22, 0(R1)	use v22 to test decoder
				470			
				471	LGF	R1, V3ADDR	load v3 source
				472	VL	v23, 0(R1)	use v23 to test decoder
				473			
				474	&INST	V22, V22, V23, &I4	test instruction (dest is a source)
				475	VST	V22, V10&TNUM	save v1 output
				476			
				477	BR	R11	return
				478			
				479	RE&TNUM	DC OF	xl16 expected result
				480			
				481	DROP	R5	
				482	MEND		
				484	*		
				485	*	macro to generate table of pointers to individual tests	
				486	*		
				487		MACRO	
				488		PTTABLE	
				489		GBLA &TNUM	
				490		LCLA &CUR	
				491	&CUR	SETA 1	
				492	. *		
				493	TTABLE	DS OF	
				494	. LOOP	ANOP	
				495	. *		
				496		DC A(T&CUR)	
				497	. *		
				498	&CUR	SETA &CUR+1	
				499	AIF	(&CUR LE &TNUM) . LOOP	
				500	*		
				501	DC	A(0)	END OF TABLE
				502	DC	A(0)	
				503	. *		
				504	MEND		
				505			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				507 *****	
				508 * E7 VRI-d tests	
				509 *****	
				510 PRINT DATA	
				511	
				512 * E777 VSLDB - Vector Shift Left Double By Byte	
				513	
				514 * VRI-d instruction, i4	
				515 * followed by	
				516 * 16 byte expected result (V1)	
				517 * 16 byte V2 source	
				518 * 16 byte V3 source	
				519 * -----	
				520 * VSLDB - Vector Shift Left Double By Byte	
				521 * -----	
				522	
				523 VRI_D VSLDB, 0	
000010B8				524+ DS OFD	
000010B8		000010B8		525+ USING *, R5	base for test data and test routine
000010B8	000010F8			526+T1 DC A(X1)	address of test routine
000010BC	0001			527+ DC H' 1'	test number
000010BE	00			528+ DC X' 00'	
000010BF	00			529+ DC HL1' 0'	i4 field
000010C0	E5E2D3C4 C2404040			530+ DC CL8' VSLDB'	instruction name
000010C8	00001130			531+ DC A(RE1+16)	address of v2 source
000010CC	00001140			532+ DC A(RE1+32)	address of v3 source
000010D0	00000010			533+ DC A(16)	result length
000010D4	00001120			534+REA1 DC A(RE1)	result address
000010D8	00000000 00000000			535+ DS FD	gap
000010E0	00000000 00000000			536+V101 DS XL16	V1 output
000010E8	00000000 00000000				
000010F0	00000000 00000000			537+ DS FD	gap
				538+*	
000010F8				539+X1 DS OF	
000010F8	E310 5010 0014	00000010		540+ LGF R1, V2ADDR	load v2 source
000010FE	E761 0000 0806	00000000		541+ VL v22, 0(R1)	use v22 to test decoder
00001104	E310 5014 0014	00000014		542+ LGF R1, V3ADDR	load v3 source
0000110A	E771 0000 0806	00000000		543+ VL v23, 0(R1)	use v23 to test decoder
00001110	E766 7000 0E77			544+ VSLDB V22, V22, V23, 0	test instruction (dest is a source)
00001116	E760 5028 080E	000010E0		545+ VST V22, V101	save v1 output
0000111C	07FB			546+ BR R11	return
00001120				547+RE1 DC OF	xl16 expected result
00001120				548+ DROP R5	
00001120	FFFFFFFF FFFFFFFF			549 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00001128	FFFFFFFF FFFFFFFF				
00001130	FFFFFFFF FFFFFFFF		550	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001138	FFFFFFFF FFFFFFFF				
00001140	00000000 00000000		551	DC XL16' 0000000000000000 0000000000000000'	v3
00001148	00000000 00000000				
				552	
				553 VRI_D VSLDB, 3	
00001150				554+ DS OFD	
00001150		00001150		555+ USING *, R5	base for test data and test routine
00001150	00001190			556+T2 DC A(X2)	address of test routine
00001154	0002			557+ DC H' 2'	test number
00001156	00			558+ DC X' 00'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001157	03			559+	DC	HL1' 3'	i4 field
00001158	E5E2D3C4 C2404040			560+	DC	CL8' VSLDB'	instruction name
00001160	000011C8			561+	DC	A(RE2+16)	address of v2 source
00001164	000011D8			562+	DC	A(RE2+32)	address of v3 source
00001168	00000010			563+	DC	A(16)	result length
0000116C	000011B8			564+REA2	DC	A(RE2)	result address
00001170	00000000 00000000			565+	DS	FD	gap
00001178	00000000 00000000			566+V102	DS	XL16	V1 output
00001180	00000000 00000000						
00001188	00000000 00000000			567+	DS	FD	gap
				568+*			
00001190				569+X2	DS	0F	
00001190	E310 5010 0014		00000010	570+	LGF	R1, V2ADDR	load v2 source
00001196	E761 0000 0806		00000000	571+	VL	v22, 0(R1)	use v22 to test decoder
0000119C	E310 5014 0014		00000014	572+	LGF	R1, V3ADDR	load v3 source
000011A2	E771 0000 0806		00000000	573+	VL	v23, 0(R1)	use v23 to test decoder
000011A8	E766 7003 0E77			574+	VSLDB	V22, V22, V23, 3	test instruction (dest is a source)
000011AE	E760 5028 080E		00001178	575+	VST	V22, V102	save v1 output
000011B4	07FB			576+	BR	R11	return
000011B8				577+RE2	DC	0F	xl16 expected result
000011B8				578+	DROP	R5	
000011B8	FFFFFFFF FFFFFFFF			579	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFF000000'	result t
000011C0	FFFFFFFF FF000000						
000011C8	FFFFFFFF FFFFFFFF			580	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000011D0	FFFFFFFF FFFFFFFF						
000011D8	00000000 00000000			581	DC	XL16' 0000000000000000 0000000000000000'	v3
000011E0	00000000 00000000						
				582			
				583	VRI_D	VSLDB, 7	
000011E8				584+	DS	0FD	
000011E8		000011E8		585+	USING	*, R5	base for test data and test routine
000011E8	00001228			586+T3	DC	A(X3)	address of test routine
000011EC	0003			587+	DC	H' 3'	test number
000011EE	00			588+	DC	X' 00'	
000011EF	07			589+	DC	HL1' 7'	i4 field
000011F0	E5E2D3C4 C2404040			590+	DC	CL8' VSLDB'	instruction name
000011F8	00001260			591+	DC	A(RE3+16)	address of v2 source
000011FC	00001270			592+	DC	A(RE3+32)	address of v3 source
00001200	00000010			593+	DC	A(16)	result length
00001204	00001250			594+REA3	DC	A(RE3)	result address
00001208	00000000 00000000			595+	DS	FD	gap
00001210	00000000 00000000			596+V103	DS	XL16	V1 output
00001218	00000000 00000000						
00001220	00000000 00000000			597+	DS	FD	gap
				598+*			
00001228				599+X3	DS	0F	
00001228	E310 5010 0014		00000010	600+	LGF	R1, V2ADDR	load v2 source
0000122E	E761 0000 0806		00000000	601+	VL	v22, 0(R1)	use v22 to test decoder
00001234	E310 5014 0014		00000014	602+	LGF	R1, V3ADDR	load v3 source
0000123A	E771 0000 0806		00000000	603+	VL	v23, 0(R1)	use v23 to test decoder
00001240	E766 7007 0E77			604+	VSLDB	V22, V22, V23, 7	test instruction (dest is a source)
00001246	E760 9010 080E		00001210	605+	VST	V22, V103	save v1 output
0000124C	07FB			606+	BR	R11	return
00001250				607+RE3	DC	0F	xl16 expected result
00001250				608+	DROP	R5	
00001250	FFFFFFFF FFFFFFFF			609	DC	XL16' FFFFFFFFFFFFFFFFFF FF00000000000000'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001258	FF000000 00000000						
00001260	FFFFFFFF FFFFFFFF			610	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001268	FFFFFFFF FFFFFFFF						
00001270	00000000 00000000			611	DC	XL16' 0000000000000000 0000000000000000'	v3
00001278	00000000 00000000						
				612			
				613	VRI_D	VSLDB, 8	
00001280				614+	DS	0FD	
00001280		00001280		615+	USING	*, R5	base for test data and test routine
00001280	000012C0			616+T4	DC	A(X4)	address of test routine
00001284	0004			617+	DC	H' 4'	test number
00001286	00			618+	DC	X' 00'	
00001287	08			619+	DC	HL1' 8'	i4 field
00001288	E5E2D3C4 C2404040			620+	DC	CL8' VSLDB'	instruction name
00001290	000012F8			621+	DC	A(RE4+16)	address of v2 source
00001294	00001308			622+	DC	A(RE4+32)	address of v3 source
00001298	00000010			623+	DC	A(16)	result length
0000129C	000012E8			624+REA4	DC	A(RE4)	result address
000012A0	00000000 00000000			625+	DS	FD	gap
000012A8	00000000 00000000			626+V104	DS	XL16	V1 output
000012B0	00000000 00000000						
000012B8	00000000 00000000			627+	DS	FD	gap
				628+*			
000012C0				629+X4	DS	0F	
000012C0	E310 5010 0014		00000010	630+	LGF	R1, V2ADDR	load v2 source
000012C6	E761 0000 0806		00000000	631+	VL	v22, 0(R1)	use v22 to test decoder
000012CC	E310 5014 0014		00000014	632+	LGF	R1, V3ADDR	load v3 source
000012D2	E771 0000 0806		00000000	633+	VL	v23, 0(R1)	use v23 to test decoder
000012D8	E766 7008 0E77			634+	VSLDB	V22, V22, V23, 8	test instruction (dest is a source)
000012DE	E760 5028 080E		000012A8	635+	VST	V22, V104	save v1 output
000012E4	07FB			636+	BR	R11	return
000012E8				637+RE4	DC	0F	xl16 expected result
000012E8				638+	DROP	R5	
000012E8	FFFFFFFF FFFFFFFF			639	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF08'	result
000012F0	FFFFFFFF FFFFFFFF08						
000012F8	FFFFFFFF FFFFFFFF			640	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001300	FFFFFFFF FFFFFFFF						
00001308	FFFFFFFF FFFFFFFF08			641	DC	XL16' FFFFFFFFFFFFFFFFFF08 FFFFFFFFFFFFFFFFFF'	v3
00001310	FFFFFFFF FFFFFFFF						
				642			
				643	VRI_D	VSLDB, 15	
00001318				644+	DS	0FD	
00001318		00001318		645+	USING	*, R5	base for test data and test routine
00001318	00001358			646+T5	DC	A(X5)	address of test routine
0000131C	0005			647+	DC	H' 5'	test number
0000131E	00			648+	DC	X' 00'	
0000131F	0F			649+	DC	HL1' 15'	i4 field
00001320	E5E2D3C4 C2404040			650+	DC	CL8' VSLDB'	instruction name
00001328	00001390			651+	DC	A(RE5+16)	address of v2 source
0000132C	000013A0			652+	DC	A(RE5+32)	address of v3 source
00001330	00000010			653+	DC	A(16)	result length
00001334	00001380			654+REA5	DC	A(RE5)	result address
00001338	00000000 00000000			655+	DS	FD	gap
00001340	00000000 00000000			656+V105	DS	XL16	V1 output
00001348	00000000 00000000						
00001350	00000000 00000000			657+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				658+*				
00001358				659+X5	DS	0F		
00001358	E310 5010 0014		00000010	660+	LGF	R1, V2ADDR	load v2 source	
0000135E	E761 0000 0806		00000000	661+	VL	v22, 0(R1)	use v22 to test decoder	
00001364	E310 5014 0014		00000014	662+	LGF	R1, V3ADDR	load v3 source	
0000136A	E771 0000 0806		00000000	663+	VL	v23, 0(R1)	use v23 to test decoder	
00001370	E766 700F 0E77			664+	VSLDB	V22, V22, V23, 15	test instruction (dest is a source)	
00001376	E760 5028 080E		00001340	665+	VST	V22, V105	save v1 output	
0000137C	07FB			666+	BR	R11	return	
00001380				667+RE5	DC	0F	xl16 expected result	
00001380				668+	DROP	R5		
00001380	0FFFFFFF FFFFFFFF			669	DC	XL16' 0FFFFFFF0FFFFFFF 08FFFFFFF0FFFFFF'	result t	
00001388	08FFFFFF FFFFFFFF							
00001390	00010203 04050607			670	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00001398	08090A0B 0C0D0E0F							
000013A0	FFFFFFFF FFFFFFF08			671	DC	XL16' FFFFFFFF0FFFFFFF08 FFFFFFFF0FFFFFFF'	v3	
000013A8	FFFFFFFF FFFFFFFF							
				672				
				673 *	Ignore: Bits 0-3 of the fourth operand should contain			
				674 *	zeros; otherwise the results are unpredictable.			
				675 *				
				676 *	VRI_D	VSLDB, 16		
				677 *	DC	XL16' FFFFFFFF0FFFFFFF FFFFFFFF0FFFFFFF'	result t	
				678 *	DC	XL16' FFFFFFFF0FFFFFFF FFFFFFFF0FFFFFFF'	v2	
				679 *	DC	XL16' F0E0D0C0B0A09010 7060504030201000'	v3	
				680 *				
				681 *	VRI_D	VSLDB, 17		
				682 *	DC	XL16' FFFFFFFF0FFFFFFF FFFFFFFF0FFFFFFF0'	result t	
				683 *	DC	XL16' FFFFFFFF0FFFFFFF FFFFFFFF0FFFFFFF'	v2	
				684 *	DC	XL16' F0E0D0C0B0A09010 7060504030201000'	v3	
				685 *				
				686 *	VRI_D	VSLDB, 48		
				687 *	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	result t	
				688 *	DC	XL16' F0E0D0C0B0A09080 7060504030201000'	v2	
				689 *	DC	XL16' 000000000000000030 0000000000000000'	v3	
				690				
				691				
000013B0	00000000			692	DC	F' 0'	END OF TABLE	
000013B4	00000000			693	DC	F' 0'		
				694 *				
				695 *	table of pointers to individual load test			
				696 *				
000013B8				697 E7TESTS	DS	0F		
				698	PTTABLE			
000013B8				699+TTABLE	DS	0F		
000013B8	000010B8			700+	DC	A(T1)		
000013BC	00001150			701+	DC	A(T2)		
000013C0	000011E8			702+	DC	A(T3)		
000013C4	00001280			703+	DC	A(T4)		
000013C8	00001318			704+	DC	A(T5)		
				705+*				
000013CC	00000000			706+	DC	A(0)	END OF TABLE	
000013D0	00000000			707+	DC	A(0)		
				708				
000013D4	00000000			709	DC	F' 0'	END OF TABLE	
000013D8	00000000			710	DC	F' 0'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				712	*****
				713	* Register equates
				714	*****
		00000000	00000001	716 R0	EQU 0
		00000001	00000001	717 R1	EQU 1
		00000002	00000001	718 R2	EQU 2
		00000003	00000001	719 R3	EQU 3
		00000004	00000001	720 R4	EQU 4
		00000005	00000001	721 R5	EQU 5
		00000006	00000001	722 R6	EQU 6
		00000007	00000001	723 R7	EQU 7
		00000008	00000001	724 R8	EQU 8
		00000009	00000001	725 R9	EQU 9
		0000000A	00000001	726 R10	EQU 10
		0000000B	00000001	727 R11	EQU 11
		0000000C	00000001	728 R12	EQU 12
		0000000D	00000001	729 R13	EQU 13
		0000000E	00000001	730 R14	EQU 14
		0000000F	00000001	731 R15	EQU 15
				733	*****
				734	* Register equates
				735	*****
		00000000	00000001	737 V0	EQU 0
		00000001	00000001	738 V1	EQU 1
		00000002	00000001	739 V2	EQU 2
		00000003	00000001	740 V3	EQU 3
		00000004	00000001	741 V4	EQU 4
		00000005	00000001	742 V5	EQU 5
		00000006	00000001	743 V6	EQU 6
		00000007	00000001	744 V7	EQU 7
		00000008	00000001	745 V8	EQU 8
		00000009	00000001	746 V9	EQU 9
		0000000A	00000001	747 V10	EQU 10
		0000000B	00000001	748 V11	EQU 11
		0000000C	00000001	749 V12	EQU 12
		0000000D	00000001	750 V13	EQU 13
		0000000E	00000001	751 V14	EQU 14
		0000000F	00000001	752 V15	EQU 15
		00000010	00000001	753 V16	EQU 16
		00000011	00000001	754 V17	EQU 17
		00000012	00000001	755 V18	EQU 18
		00000013	00000001	756 V19	EQU 19
		00000014	00000001	757 V20	EQU 20
		00000015	00000001	758 V21	EQU 21

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	5084	0000- 13DB	0000- 13DB
Regi on		5084	0000- 13DB	0000- 13DB
CSECT	ZVE7TST	5084	0000- 13DB	0000- 13DB

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-20-VSLDB.asm
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**** NO ERRORS FOUND ****